AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-24, without prejudice. Please add new claims 25-37 , as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1 – 24 (cancelled)

Claim 25 (new): A stacked-chip semiconductor device comprising:

an interposer substrate; and

a plurality of semiconductor chips overlaid two tiers deep or more and mounted on said interposer chip, wherein

at least one of said semiconductor chips has a thick-film wiring, and at least one voltage selected from power supply voltage and ground is fed from said interposer substrate by way of said thick-film wiring to a circuit surface of another semiconductor chip that is disposed above said semiconductor chip.

Claim 26 (new): The stacked-chip semiconductor device according to claim 25, said plurality of semiconductor chips being composed of: a first semiconductor chip that has a circuit surface on an upper surface and said thick-film wiring; and a second semiconductor chip that is disposed above said first semiconductor chip and that has a plurality of through-wires and a circuit surface on an upper surface, comprising:

a plurality of bumps for providing an electrical connection between said plurality of through-wires and said thick-film wiring; and

bonding wires for electrically connecting said interposer substrate and said thick-film wiring, wherein

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE,
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

at least one voltage selected from power supply voltage and ground is fed from said interposer substrate to the circuit surface of said second semiconductor chip by way of said bonding wires, said thick-film wiring, said plurality of bumps, and said plurality of through-wires.

Claim 27 (new): The stacked-chip semiconductor device according to claim 25, said plurality of semiconductor chips being composed of: a first semiconductor chip that has a circuit surface on an upper surface and said thick-film wiring; and a second semiconductor chip that is disposed above said first semiconductor chip and that has said plurality of through-wires and a circuit surface on a lower surface, comprising:

a plurality of bumps for providing an electrical connection between said second semiconductor chip and said thick-film wiring;

bonding wires for electrically connecting said interposer substrate and said thick-film wiring; and

other bonding wires for providing an electrical connection between said interposer substrate and said second semiconductor chip,

wherein a power supply voltage and ground are fed from said interposer substrate to the circuit surface of said second semiconductor chip by way of said bonding wire, said thick-film wiring, and said plurality of bumps, and

electrical signals are transmitted between the circuit surface of said second semiconductor chip and said interposer substrate by way of said plurality of through-wires and said other bonding wires.

Claim 28 (new): The stacked-chip semiconductor device according to claim 25, wherein a spacer formed with through-wires is disposed between said semiconductor chip and said other

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE,
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

semiconductor chip, and at least one voltage selected from power supply voltage and ground is fed from said interposer substrate by way of said thick-film wiring and said through-wire to the circuit surface of another semiconductor chip.

Claim 29 (new): The stacked-chip semiconductor device according to claim 26, wherein the thickness of said thick-film wiring is the same as the height of said plurality of bumps.

Claim 30 (new): The stacked-chip semiconductor device according to claim 29, wherein said thick-film wiring and said plurality of bumps are formed by plating.

Claim 31 (new): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a plurality of through-wires;

a second semiconductor chip that is disposed above said first semiconductor chip and that has a circuit surface on a lower surface;

a first conducting member that feeds at least one voltage selected from power supply voltage and ground to a circuit surface of said first semiconductor chip; and

a second conducting member that feeds at least one voltage selected from power supply voltage and ground to said circuit surface of said second semiconductor chip,

wherein said first conductive member and said second conductive member are mutually independent routes.

Claim 32 (new): The stacked-chip semiconductor device according to claim 31, wherein the second conducting member that feeds a power supply voltage and ground to the circuit surface of said second semiconductor chip has a plurality of through-wires disposed on said first semiconductor chip, and at least one voltage selected from power supply voltage and ground is

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE,
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

fed from said interposer substrate to the circuit surface of said second semiconductor chip by way of said plurality of through-wires.

Claim 33 (new): The stacked-chip semiconductor device according to claim 32, wherein a spacer that has a plurality of through-wires is disposed between said first semiconductor chip and said second semiconductor chip, and at least one voltage selected from power supply voltage and ground is fed from maid interpomer substrate by way of the through-wires of said first semiconductor chip and the through-wires of said spacer to the circuit surface of second semiconductor chip.

Claim 34 (new): The stacked-chip semiconductor device according to claim 32, wherein the first conducting member that feeds a power supply voltage and ground to the circuit surface of said first semiconductor chip has a thick-film wiring disposed on said first semiconductor chip, and at least one voltage selected from power supply voltage and ground is fed from said interposer substrate to the circuit surface of said first semiconductor chip by way of said thick-film wiring.

Claim 35 (new): The stacked-chip semiconductor device according to claim 33, comprising:

a plurality of first bumps for electrically connecting the plurality of through-wires of said first semiconductor chip and said interposer substrate; and

a plurality of second bumps for electrically connecting the plurality of through-wires of said first semiconductor chip and said second semiconductor chip.

Claim 36 (new): The stacked-chip semiconductor device according to claim 35, wherein said thick-film wiring of said first semiconductor chip is disposed on a lower surface of said first semiconductor chip, and the thickness of said thick-film wiring is the same as the height of said first bumps.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE,
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Claim 37 (new): The stacked-chip semiconductor device according to claim 35, wherein said thick-film wiring of said first semiconductor chip is disposed on an upper surface of said first semiconductor chip, and the thickness of said thick-film wiring is the same as the height of said second bumps.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE,
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567